Dean&Francis
ISSN 2959-6157

A Review of the Synergistic Research on Materials, Physics, and Reliability of Wide Bandgap Semiconductor (SiC/GaN) Power Devices

Chengwei Zhang

School of Mathematics and Physics, University of Science and Technology Beijing, Beijing, China
u202240157@xs.ustb.edu.cn

Abstract:

Wide bandgap semiconductors (SiC/GaN) are becoming the core materials for next-generation power devices due to their high breakdown field strength, high thermal conductivity, and high-frequency characteristics. They play a crucial role in efficient energy conversion applications such as electric vehicles and photovoltaic inverters. However, their performance and reliability are constrained by material defects (such as micropipes and dislocations in SiC, and interface states in GaN), device physical mechanisms (such as gate oxide degradation and current collapse), and failure issues under complex operating conditions. This paper systematically analyzes the synergistic relationship between material properties, device physics, and reliability, proposing solutions to key challenges through multi-dimensional synergistic mechanisms, such as NO annealing interface optimization of SiC and Fe co-doping trap engineering of GaN. It also suggests enhancing device performance through physical model correction and process innovation. The study shows that the full-chain optimization of structure-material-process-system is essential for advancing wide bandgap power devices towards higher reliability, greater power, and lower costs. Future research will focus on large-scale substrate preparation, precise control of interface states, and reliability verification under extreme operating conditions to further expand their application potential .

Keywords: Wide bandgap semiconductor; SiC/GaN power device; reliability; collaborative optimization.

1. Introduction

The global energy revolution, driven by the rapid development of renewable energy, electric vehicles, and smart grids, has created an urgent need for high-efficiency power electronic devices. Traditional silicon-based power devices have reached their physical limits in terms of breakdown voltage, switching frequency, and operating temperature, which hinders further improvements in energy conversion efficiency. Wide bandgap semiconductor materials, such as silicon carbide (SiC) and gallium nitride (GaN), have emerged as ideal alternatives due to their superior material properties: a critical breakdown field strength 3-10 times higher than silicon, a thermal conductivity 3-5 times higher than silicon, and a faster electron saturation rate [1][2]. These advantages enable SiC/GaN power devices to achieve higher power density, faster switching speeds, and lower energy losses, making them particularly suitable for high-voltage, high-frequency, and high-temperature applications in electric vehicles, photovoltaic inverters, and industrial power systems.

However, the performance and reliability of SiC/GaN devices are still constrained by material defects (such as micropipes and dislocations in SiC, and interface states in GaN), physical challenges (such as gate oxide degradation in SiC MOSFETs and current collapse in GaN HEMTs), and complex failure mechanisms under harsh operating conditions. For example, defects in SiC can create leakage paths, reducing the breakdown voltage, while traps at the GaN heterojunction interface can degrade the mobility of the two-dimensional electron gas (2DEG), leading to a decrease in dynamic on-resistance. These issues highlight the intrinsic link between material properties, device physics, and reliability, necessitating a systematic approach to address them collaboratively.

This study systematically explores the synergistic mechanisms of material properties, device physics, and reliability in SiC/GaN power devices. The core objectives include: (1) analyzing how material defects affect device physical properties, such as gate oxide defect-assisted tunneling and dynamic resistance caused by traps; (2) revealing the relationship between device structure (such as terminal protection design and integrated modules) and long-term reliability; (3) proposing cross-dimensional optimization strategies, including defect engineering (such as NO annealing at the SiC/SiO2 interface and Fe co-doping in the GaN buffer layer), physical-based model correction (such as dynamic resistance models with traps), and process innovation (such as edge terminal technology). By establishing a “material-physics-reliability” collaborative design framework, the existing technical bottleneck is broken through, and a path is provided for the development of next-generation power devices with higher reliability, greater power and lower cost.

The research results will provide theoretical and practical guidance for the development of SiC/GaN technology, accelerate its application in efficient energy systems, and contribute to the global sustainable energy transition.

2. Material Characteristics and Defects: SiC vs GaN

2.1 SiC Material Characteristics

SiC is a wide-bandgap semiconductor material with various crystal structures. However, during the growth of SiC crystals, defects such as micropipes, basal plane dislocations, and screw dislocations can easily occur. Micropipes, which are hollow tubular defects that run through the crystal, can cause localized electric field concentration in devices, significantly reducing the breakdown voltage and increasing leakage current. Basal plane dislocations may transform into stacking faults when bipolar devices operate, leading to increased on-resistance and long-term reliability issues [3]. The performance advantages of SiC materials are limited by their crystal defects, so reducing the density of these defects is crucial for enhancing the performance of SiC devices.

2.2 GaN Material Characteristics

GaN Devices are typically grown heteroepitaxially on substrates of Si and SiC. Due to lattice mismatch and differences in thermal expansion coefficients, the epitaxial layer can develop stress, leading to cracks that affect device efficiency. This issue can be mitigated by inserting a stress buffer layer. The core advantage of GaN devices lies in the two-dimensional electron gas (2DEG) formed at the heterojunction interface [4]. The high concentration and mobility of this gas result in low on-resistance. However, interface states scatter carriers, reducing the mobility of the 2DEG and causing dynamic performance degradation issues such as current collapse [5].

2.3 The Correlation Between Materials and Device Performance

In SiC, microtubules and dislocations can form leakage paths, increasing reverse leakage current and reducing the breakdown voltage. Interface states at the SiC/SiO2 interface lead to low channel mobility in MOSFETs, which requires improvement through nitrogen passivation. In GaN, roughness or impurities at the heterojunction interface can reduce the mobility of 2DEG and cause threshold voltage drift. Optimizing epitaxial growth processes and interface

ISSN 2959-6157

treatments is crucial for enhancing device reliability.

3. Device Physical Mechanism and Key Structure Design

3.1 Mainstream Device Structure

SiC power devices, such as MOSFETs, feature a vertical conductive structure that utilizes the high breakdown field strength of SiC to achieve high-voltage characteristics. However, the interface states at the SiC/SiO2 interface lead to low channel mobility, necessitating the optimization of the gate oxide interface through nitrogen passivation. This process enhances high-frequency performance but poses a critical challenge in terms of gate oxide reliability. JFETs, on the other hand, avoid the gate oxide interface challenges and associated reliability issues faced by MOSFETs [6]. However, like all SiC devices, JFETs can still be affected by bulk material defects such as micropipes and dislocations (as discussed in Section 2.1), which can create leakage paths and impact breakdown voltage. And, JFETs are more complex to drive and are suitable for high-reliability applications. SBDs leverage the high critical breakdown field strength of SiC to minimize reverse recovery loss, but defects in the material, such as basal plane dislocations, can increase reverse leakage current, requiring defect control processes to improve. GaN Power devices include HEMT (High Electron Mobility Transistor), which utilizes the conductivity of a two-dimensional electron gas (2DEG) formed at the heterojunction interface to achieve ultra-low on-resistance and high-frequency switching. GaN gate devices, such as p-GaN gate HEMT, feature an enhanced design through a p-type GaN gate, but the gate interface states can cause threshold voltage drift, necessitating precise control of epitaxial doping. Hybrid devices, like the Cascode structure, combine Si MOSFETs with GaN HEMTs to simplify drive designs [7].

3.2 Core Issues of the Physical Mechanism

The reliability of the gate oxide in MOSFETs is one of the key challenges in the current power semiconductor industry, especially in high-voltage, high-temperature, and high-frequency applications. The failure of the gate oxide directly affects the device's long-term stability and lifespan. Micro-tubes and dislocations can form leakage paths, necessitating optimized substrate growth processes to reduce defect density.

The current collapse effect of the HEMT device refers to the phenomenon that the conduction current of the device temporarily decreases after the high-voltage switch is working, which is manifested by the dynamic conduction resistance significantly higher than the static value [8].

The reliability issue of gate oxide in SiC MOSFETs stems primarily from the poor quality of the SiC/SiO2 interface. Compared to traditional Si/SiO2 interfaces, the interface state density (Dit) at SiC/SiO2 interfaces is typically one to two orders of magnitude higher [9].

3.3 Current Structural Innovation and Optimization

Terminal protection structure: SiC uses JTE or field limit ring to optimize the electric field distribution and improve the breakdown voltage. GaN: Introduce a field plate or oblique terminal to suppress the edge electric field concentration.

Integrated design: single chip integration such as SiC MOSFET and SBD, co-packaging to reduce parasitic parameters; heterogeneous integration, GaN-on-Si and Si CMOS driver circuit integration to improve system efficiency.

4. Reliability Challenges and Failure Mechanisms

4.1 Failure Mode of SiC Devices

Gate Oxide Degradation:

The primary issue with the gate oxide reliability of MOSFETs is the degradation of the gate oxide under prolonged high-voltage or high-temperature stress, which manifests as threshold voltage drift, increased gate leakage current, or breakdown. The root cause lies in the high defect density at the SiC/SiO2 interface, leading to electron-hole traps. Additionally, micropipes and dislocations during SiC crystal growth increase the interface state density, necessitating nitrogen passivation to reduce leakage paths [10].

Body diode degradation:

SiC The built-in PN junction of the MOSFET degrades during continuous conduction or reverse recovery, resulting in increased forward voltage drop and higher reverse leakage current. When the body diode is conducting, electrons and holes simultaneously enter the drift region, causing the expansion of basal dislocations in the SiC lattice, leading to stacking dislocations. These dislocations impede carrier movement, increase resistance, and trigger local overheating, creating a vicious cycle.

4.2 GaN Failure Mode of Devices

Dynamic conduction resistance degradation:

After the device works in a high-voltage switch, the

on-resistance increases significantly, especially under high temperature or high-pressure stress. The defects in GaN devices capture carriers under high-pressure stress and form a space charge region, which hinders the movement of channel electrons.

Hot electron effect and gate breakdown:

Under a high electric field, electrons acquire sufficient energy to become hot electrons, which can cause irreversible damage. Electrons are accelerated in a strong electric field (such as near the drain region with high field strength), collide with the lattice, and produce ionization or defects. Hot electrons are injected into the gate dielectric or buffer layer, leading to an increase in interface states or material damage.

Gate breakdown is caused by the breakdown of the gate dielectric under high voltage, resulting in gate failure. The cause is the concentration of the electric field at the gate edge, which leads to the breakdown of the dielectric layer or the reverse piezoelectric effect. The piezoelectric properties of GaN generate mechanical stress under high electric fields, accelerating material degradation.

4.3 Test Methods and Standards

High temperature grid bias (HTGB):

SiC MOSFET can last for 1000 hours under the condition of VGS = ± 20V and

Tj =175-200℃, while GaN HEMT is VGS = +6V/-10V, Tj =150℃

High humidity and high pressure (H3TRB):

In an environment of 85℃/85%RH and rated voltage of 80-100%, the dynamic Ron of some GaN devices increased by 40% due to surface oxidation of AlGaN, while the sample with atomic layer deposition (ALD) Al2O3 packaging only increased by 5%.

5. Collaborative Optimization Mechanism of Material-Physics-Reliability

5.1 A Research Framework for Collaborative Optimization

1. Material optimization

SiC Material defect suppression: Micropipes and basal plane dislocations in SiC crystals lead to increased leakage current, which affects the reliability of the gate oxide. Low temperature epitaxial growth in situ doping can be used to reduce the dislocation density; NO annealing process passivates the interface state of SiC/ SiO_2 [11].

GaN Heterojunction optimization: GaN interface roughness and carbon impurities lead to 2DEG scattering, which leads to dynamic Ron degradation.

2. Physical model correction

SiC MOSFET gate oxide reliability model:

The traditional power-law model does not take into account the interface state-assisted tunneling, resulting in an error of up to 30% in the prediction of gate oxide lifetime. The error is reduced to 8% by introducing the distribution function of interface state density (Dit) and correcting the breakdown prediction under high field strength.

GaN HEMT dynamic resistance model:

The ASM-HEMT model does not include the trap charge-discharge effect and cannot predict the current collapse. The time constant matrix of the embedded trap is used to simulate the error with a measurement error of less than 10%.

3. Reliability Enhancement Strategies and Validation

The optimization can be achieved by Fe co-doping to compensate deep energy level traps, and ALD Al_2O_3 passivation to inhibit surface oxidation.

SiC Device: HTGB test (175℃/±20V) verified that the gate ox life was increased from 10^2 hours to 10^4 hours.

GaN Device: The pulse IV test shows that the dynamic Ron degradation rate is reduced from 40% to less than 5%, meeting the PAE requirements of 6G communication.

5.2 Case Study Analysis

Case 1: SiC/SiO2 interface state control-gate oxide physical model correction-life improvement:

Problem: The high density Dit at the interface of SiC/SiO2 is caused by traditional thermal oxidation, which leads to threshold voltage drift.

Optimization: The Si dangling bond was converted into a Si-N bond by the NO annealing process, and the interface state density Dit was reduced by 50%.

Model correction: In the classical power-law model, the interface state-assisted tunneling term is added, and the prediction error of gate oxide breakdown field strength is reduced from 30% to 8%.

Effect: The TDDB life is extended from 10^2 hours to 10^4 hours at 175℃, which meets the requirements of electric vehicle inverters [12].

Case 2: GaN trap engineering-suppression of current collapse-dynamic resistance stabilization:

Mechanism: The carbon impurity in the buffer layer forms a deep energy level trap (Ec-0.5eV), resulting in an in-

ISSN 2959-6157

crease of dynamic resistance by 300%.

Optimization: During epitaxial growth, Fe co-doping compensated carbon traps were introduced to reduce the trap density from 5×10^{17} cm^{-3} to 1×10^{16} cm^{-3}.

Verification: The pulse IV test shows that the current collapse rate is improved from 40% to 5%, and the PAE (power added efficiency) of the radio frequency device is increased by 15%.

Model upgrade: The trap charge-discharge time constant matrix is embedded in the ASM-HEMT model, and the simulation and measurement errors are less than 10% [13].

6. Frontier Advances

6.1 Recent Technological Advances

12-Inch substrate, trench gate MOSFET commercialization.

SiC Technology is rapidly advancing towards larger sizes and higher performance. The 12-inch SiC substrate has become a focal point in the industry, significantly boosting chip production efficiency and reducing costs. Valley-gate SiC MOSFETs have entered the commercialization phase, with Wolfspeed's third-generation planar technology optimizing switching losses, and Rohm's integrated modules achieving high-frequency operation at 100kHz, enhancing the performance of electric vehicles and photovoltaic inverters.

6.2 GaN: Vertical Structure Devices, Integrated Intelligent Power Modules

GaN Technology is advancing towards higher power and higher integration. GaN Devices, such as Transphorm's 175℃ automotive-grade FET, have overcome the issue of dynamic resistance stability, making them suitable for high-current applications. Navitas has introduced the world's first bidirectional GaN power IC, which integrates a drain structure and intelligent drive, simplifying the design of renewable energy and on-board charging systems, reducing the size by 30%.

6.3 Application Scenarios: Electric Vehicles, Photovoltaic Inverters

Electric vehicles: SiC MOSFET replaces silicon-based IGBT to improve inverter efficiency, GaN used for00 48V light hybrid system, supports high-density power management.

Photovoltaic inverter: SiC Module reduces switching loss, GaN, hybrid design, improves conversion efficiency to 97.8%.

7. Conclusion

Wide bandgap semiconductors SiC and GaN power devices, thanks to their superior material properties, show great potential in high-voltage, high-frequency, and high-temperature applications. However, their performance and reliability are still constrained by core issues such as material defects, interface states, and physical mechanisms. This paper systematically analyzes the material characteristics, device structure design, failure mechanisms, and collaborative optimization strategies of SiC and GaN, revealing the intrinsic relationship between materials, physics, and reliability. The study shows that significant improvements in device performance can be achieved through material defect suppression (such as NO annealing of SiC and Fe co-doping of GaN), physical model correction (such as gate oxide reliability models and dynamic resistance models), and process optimization (such as terminal protection structures and integrated design). Collaborative research not only addresses current technical bottlenecks (such as gate oxide degradation and current collapse) but also provides theoretical support for innovation throughout the entire chain.

In the future, the development of wide bandgap power devices will continue to face challenges, including cost control for large substrates, further reduction of interface states, and long-term reliability verification under extreme conditions. Through collaborative innovation across the entire chain from structure to material, process, and system, SiC and GaN devices will advance towards higher reliability, greater power, and lower costs, driving revolutionary advancements in areas such as electric vehicles and photovoltaic inverters.

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